嘉兴斯达半导体有限公司

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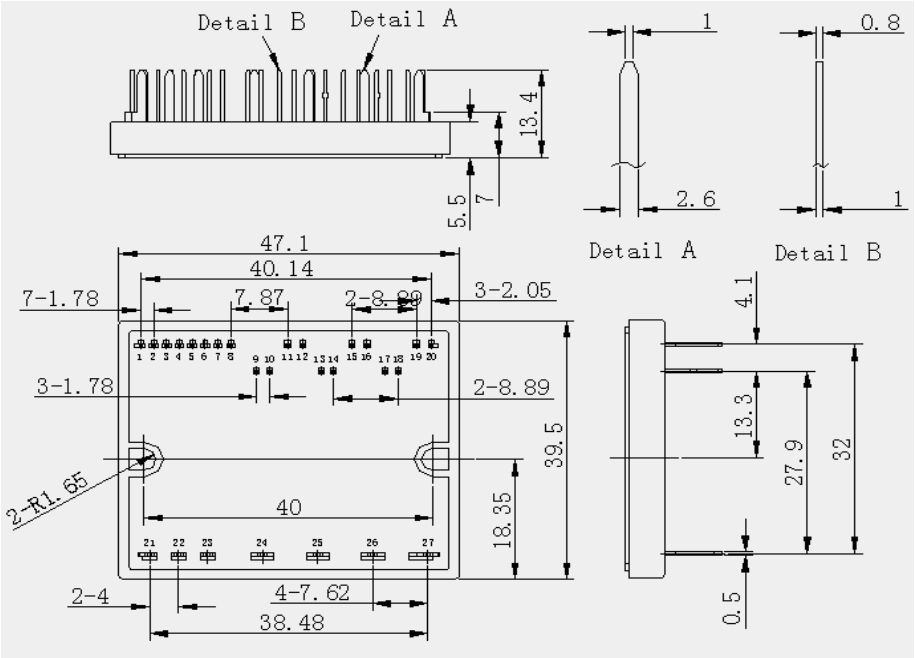
1.2.1 Drawing



TERMINAL CODE

1 VCC	15 VB(V)
2 COM	16 VS(U)
3 IN(UL)	17 IN(VL)
4 IN(VL)	18 VCC
5 IN(WL)	19 VB(W)
6 VFO	20 VS(W)
7 CFOD	21 NU
8 CSC	22 NV
9 IN(UH)	23 NW
10 VCC	24 U
11 VB(U)	25 V
12 VS(U)	26 W
13 IN(VH)	27 P
14 VCC	

Figure 1-2. Package Outlines

1.2.2 Ordering Information

ID 20 F T 06 A1 S

(1) (2) (3) (4) (5) (6) (7)

(1) Device: Intelligent Power Module
(2) Current Rating: 20=20A
(3) Circuit Configuration: F=Three Phase, P=Seven Pack
(4) Chip Characteristics: L=NPT Low Loss, T=Trench Low Loss
(5) Voltage Rating: 06=600V, 12=1200V
(6) Package Style
(7) Options

1.2.3 Starpower ID-IPM Series

Table 1-1. Starpower ID-IPM Series and General Applications

Part Number	Ratings	Motor Ratings(*)	PWM Frequency(Typ.)	Remark
ID10FT06A1S	600V/10A	0.5 KW/220Vac	15kHz	V_{iso} = AC 2500V_{rms} (Sinusoidal 1min)
ID15FT06A1S	600V/15A	0.75 KW/220Vac	15kHz	
ID20FT06A1S	600V/20A	1.5 KW/220Vac	15kHz	
ID30FT06A1S	600V/30A	2.2 KW/220Vac	15kHz	

1.3 Home appliances & Industrial application

Motor drive for household electric appliances: air conditioners, washing machines, refrigerators, low power industrial applications such as treadmill and general purpose inverter as well. IPM is the best choice for the low power motor drivers.

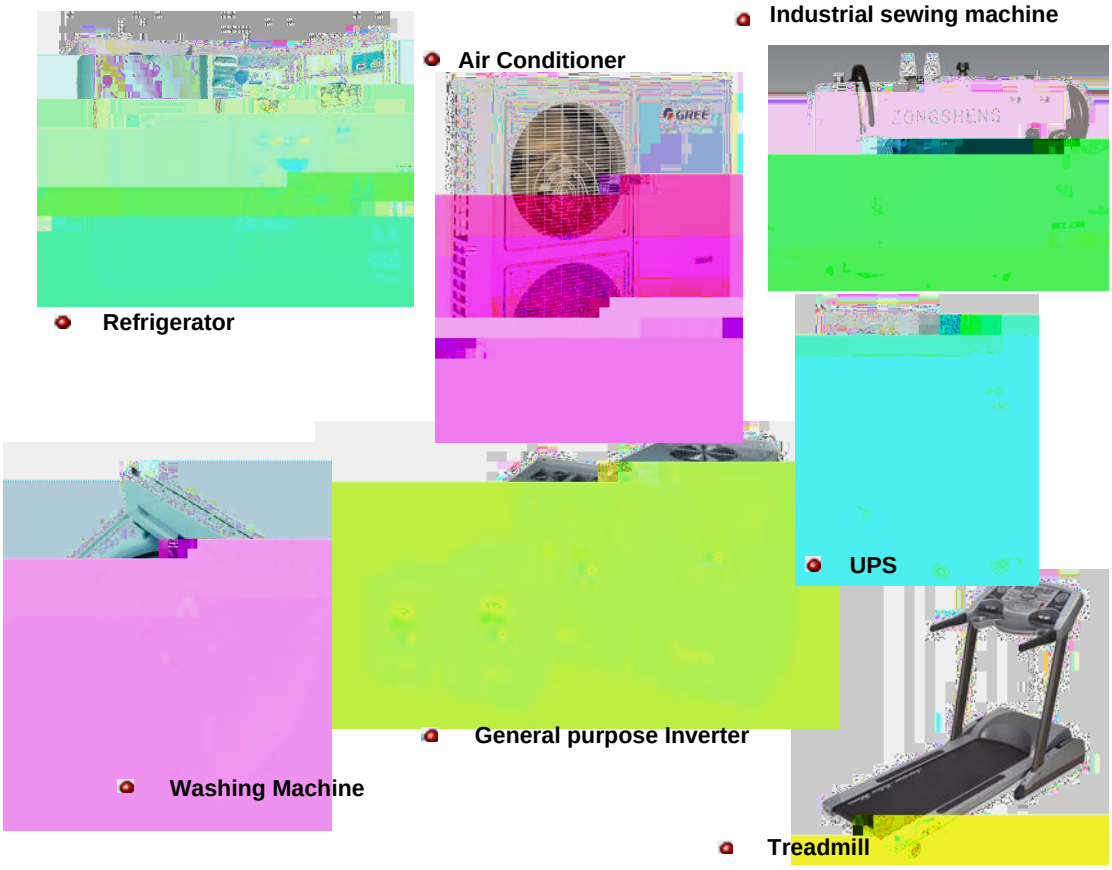


Figure 1-3. Home and industrial application areas

1.4 Internal circuit and Features

1.4.1 Internal Block Diagram

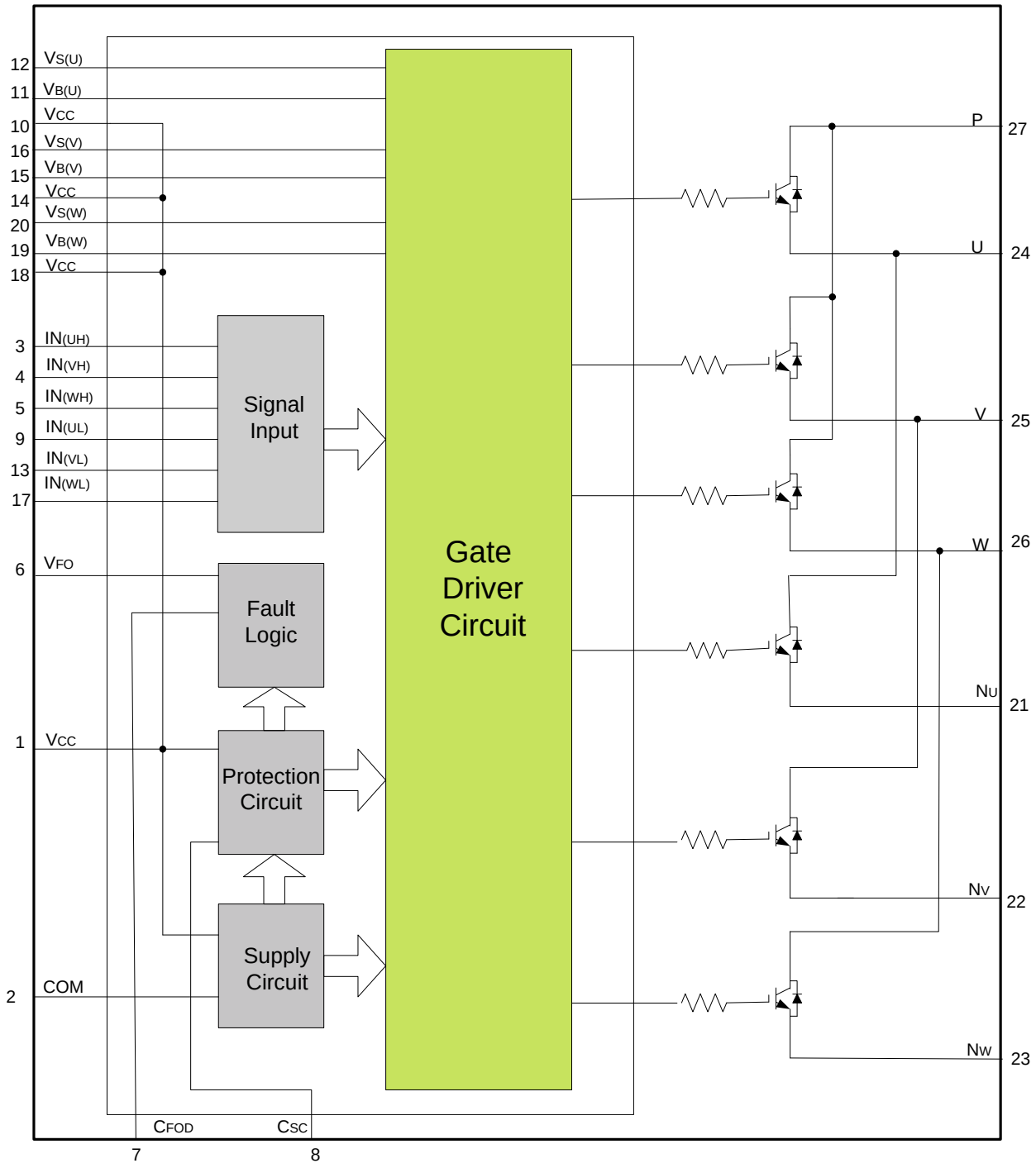
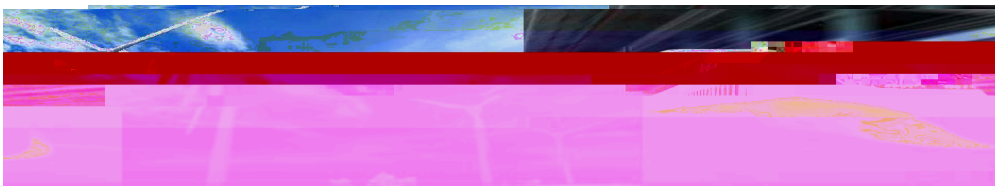


Figure1-4 Internal Block Diagram of Starpower ID IPM



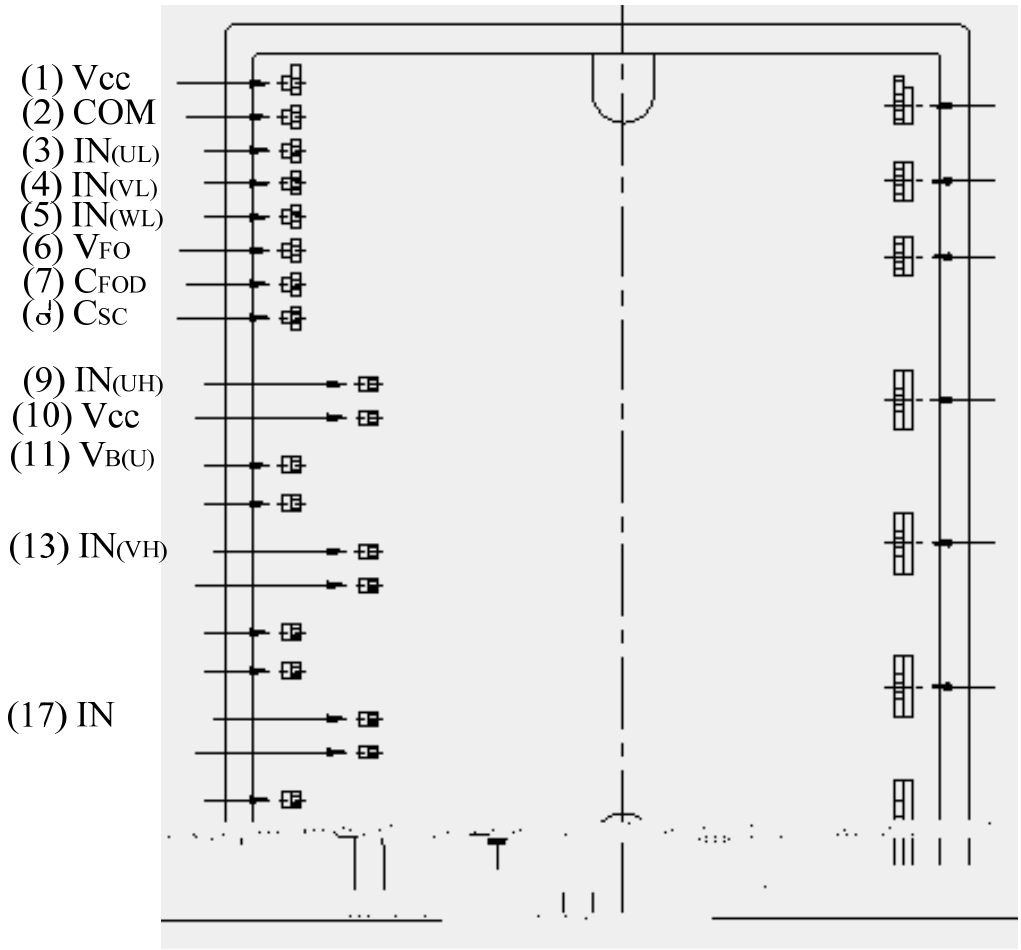
1.4.2 Features and Functions

Features

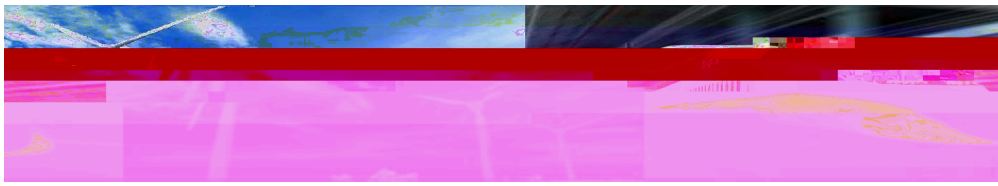
- UL Certified (UL 1557).
- Low power dissipation and excellent thermal package design.
- Low temperature coefficient effect both for driver and IGBT.
- Divided negative dc-link terminals for inverter current sharing application.
- Matched propagation delay for all channels.
- Lead-Free packaging and RoHS compatible.
- Provided a fault signal (V_{FO} pin) and shut-off internal IGBT when OC/SC and under-voltage event occur.

Chapter 2 Electrical Characteristics

2.1 Description of the Input and Output Pins



No.	Symbol	Pin Description
1	V_{CC}	Supply Voltage Terminal for Driver IC
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-side U Phase
4	$IN_{(VL)}$	Signal Input for Low-side V Phase
5	$IN_{(WL)}$	Signal Input for Low-side W Phase
6	V_{FO}	Fault Output
7	C_{FOD}	Capacitor for Fault Output Duration Time Selection
8	C_{SC}	Capacitor (Low-pass Filter) for Short-Current Detection Input



2.1.2 Pin Descrition

Supply source of the ID- IPM

Pin symbol V_{CC}

- V_{CC} is internal connected together.
- It is necessary to mount (as possible as close to these pins) a capacitor of favorable frequency to prevent malfunction caused by the unstable operation.
- To prevent damage the internal driver IC. So, it is necessary to keep the operation supply voltage below the maximum specified values.

Grounding port

Pin symbol COM

- This is the driver ground for the internal driver IC.
- Main loop current of the power circuit loop should not be allowed to flow through these terminals to avoid noise influences.

Short-circuit trip voltage sensing port

Pin symbol C_{SC}

- The designer need to insert the current sensing resistor between this terminal and GND to detect OC/SC situations.
- The port may recognize the noise as the real input, so the designer need to add a suitable RC filter to reduce the noise level but don't delay the actual signal.

Fault pulse output time setting port

Pin symbol C_{FOD}

- This port is used for setting the fault pulse output time.
- In order to set the fault pulse output time, the designer may need to add an external capacitor between this port and grounde(set g)54 26aCJ-22nnuse pingRxoun(d op)5.87 1p ng.1(ao.ort r)de(ki)6p.ort une RCfine FNotUL T o

- Active logic corresponding to the state of the IGBT.
- These pins are input port which is used to detect the controlling pattern to active the IGBT for switching.
- To put RC filter in front of the input port is recommended.
- In order to eliminate the noise when the signal level is changing its state, the trace from controller to the port is recommended as short as possible.

High-side drive supply port / High-side drive supply reference port

Pin symbol $V_{B(U)}$-$V_{S(U)}$, $V_{B(V)}$-$V_{S(V)}$, $V_{B(W)}$-$V_{S(W)}$

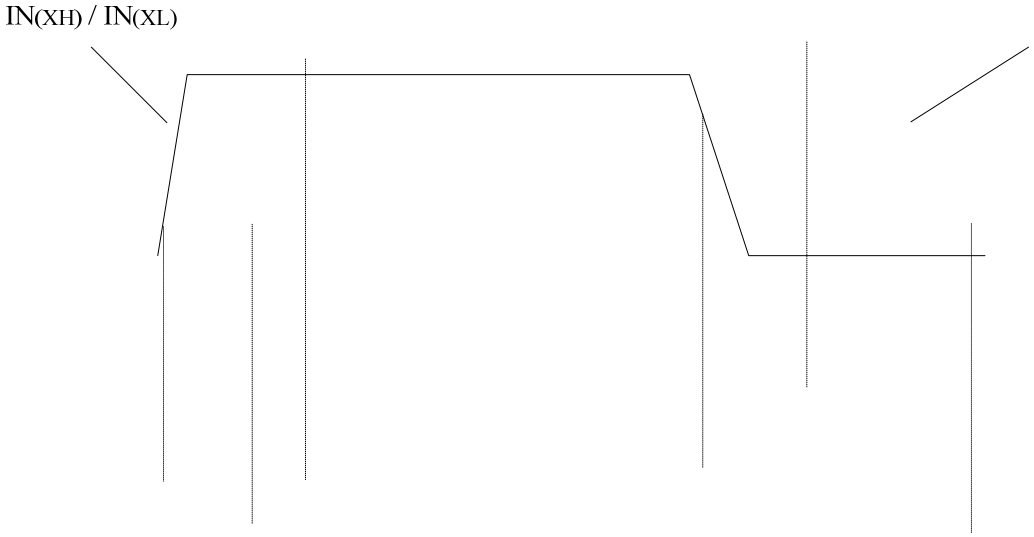
- The bootstrap circuit scheme is needed for driving high side IGBTs by using single supply source.
- B(x)-S(x) means the input voltage terminal for high-side IGBTs.
- It is necessary to mount(as possible as close to these pins) a capacitor of favorable frequency to prevent malfunction caused by the unstable operation.

Inverter positive power supply port

Pin symbol P

- DC-Link positive terminal connected to the collectors of the high-side IGBTs internally.
-

Item	Symbol	Condition	Min.	Typ.	Max.	Unit


IN(XH) / IN(XL)

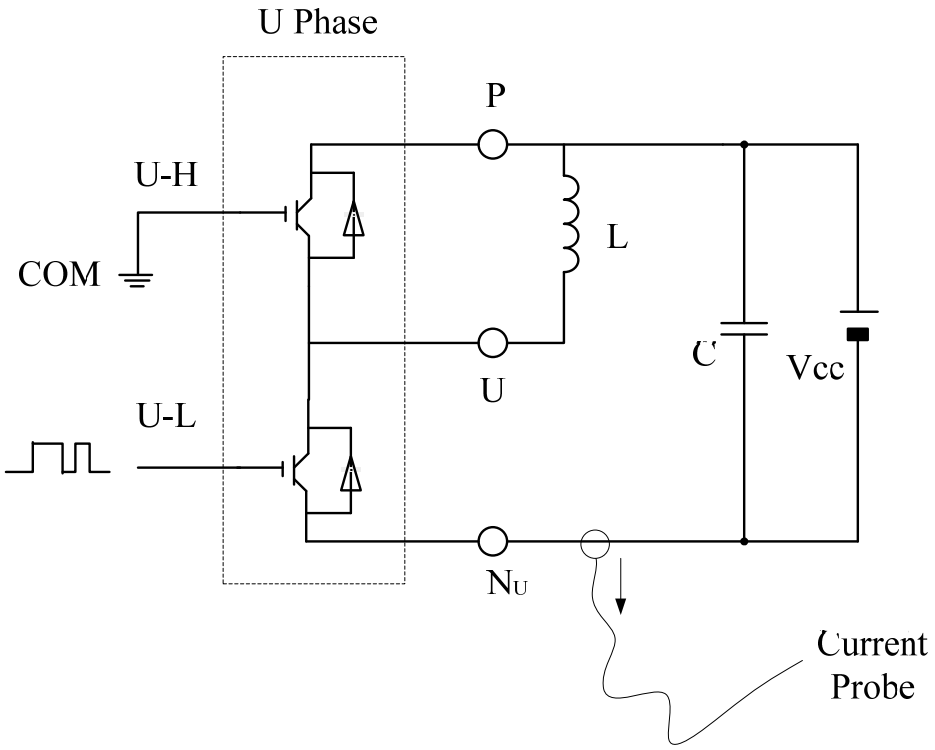


Figure 2-4. Test Circuit of Dynamic Parameter

Switching Characteristics

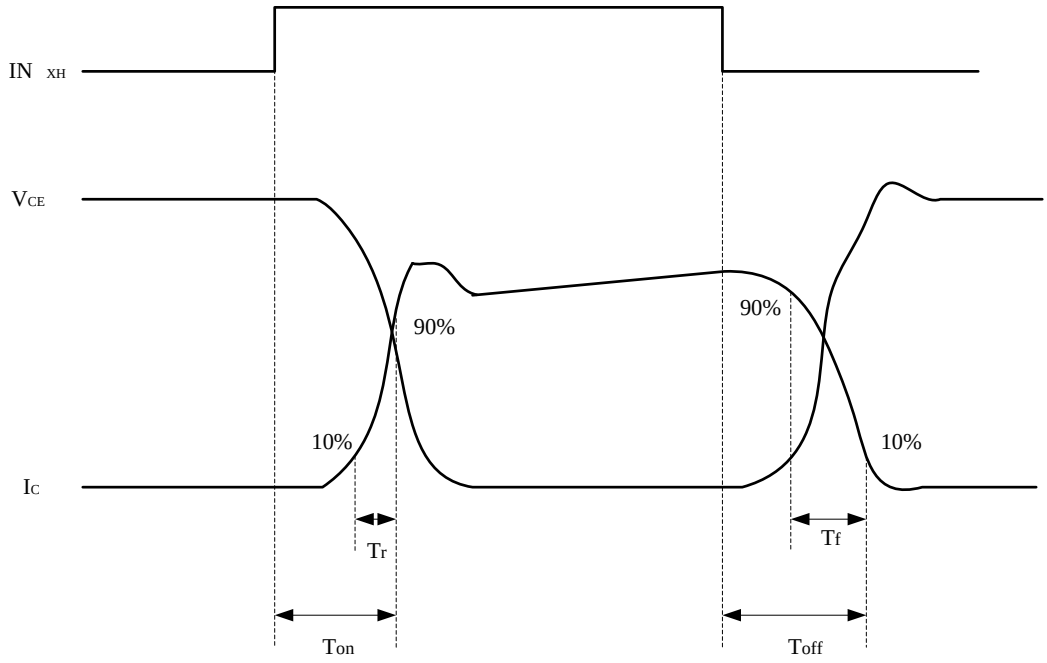
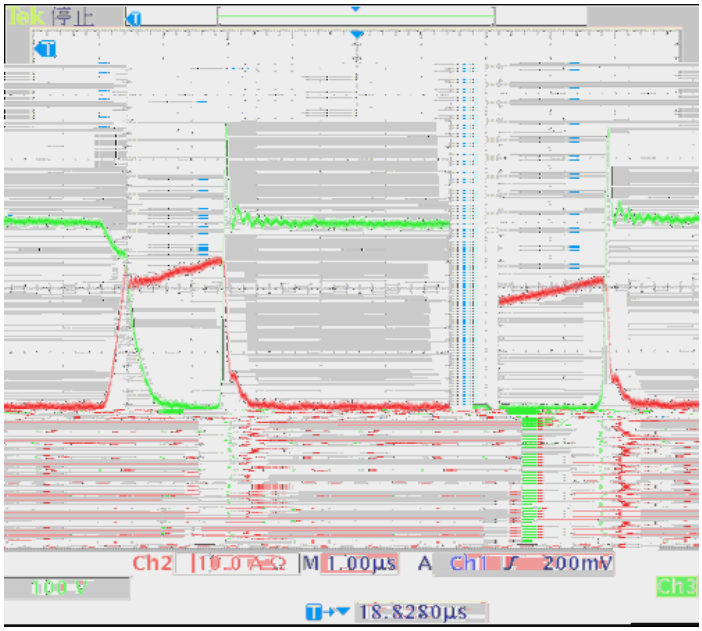
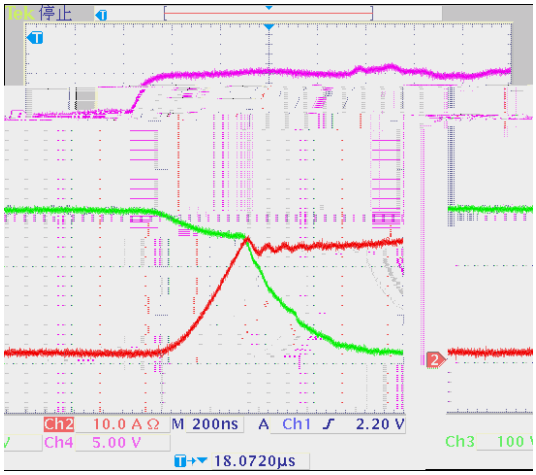


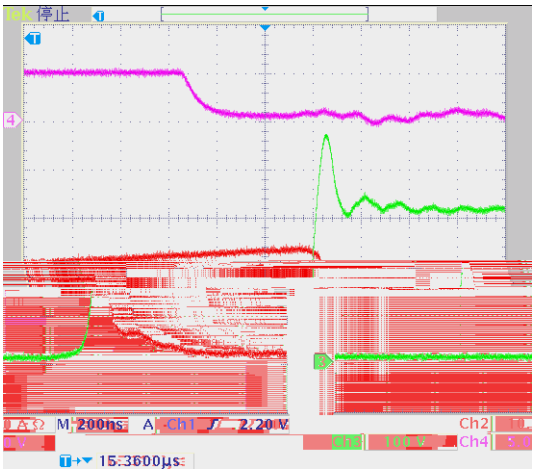
Figure 2-5. Switching Time Definition

Test Conditions V_{DC} = 300V, V_{CC} = 15V, I_C = 20A, Vin = 0V→5V, T_C = 25 , Inductive Load Circuit

Ch2: I_C
Ch3: V_{CE}

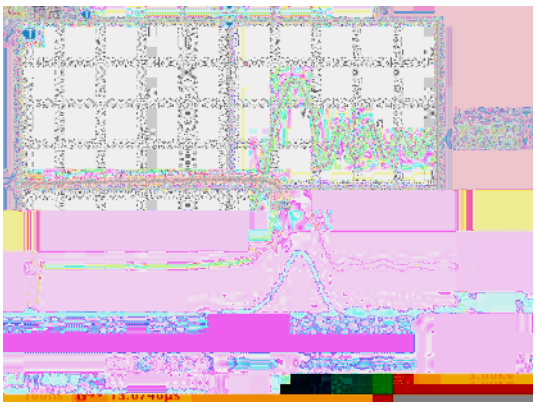






Ch2: I_C
Ch3: V_{CE}
Ch4: $IN_{(UH)}$





Ch2: I_C
Ch3: V_{CE}
M: Switching Loss

Figure 2-6. Switching Waveform of ID- IPM (Used ID20FT06A1S class) (Typ.)

Chapter 3 Packaging and Installation Guide

3.1 Package

3.1.1 Internal Structure Overview

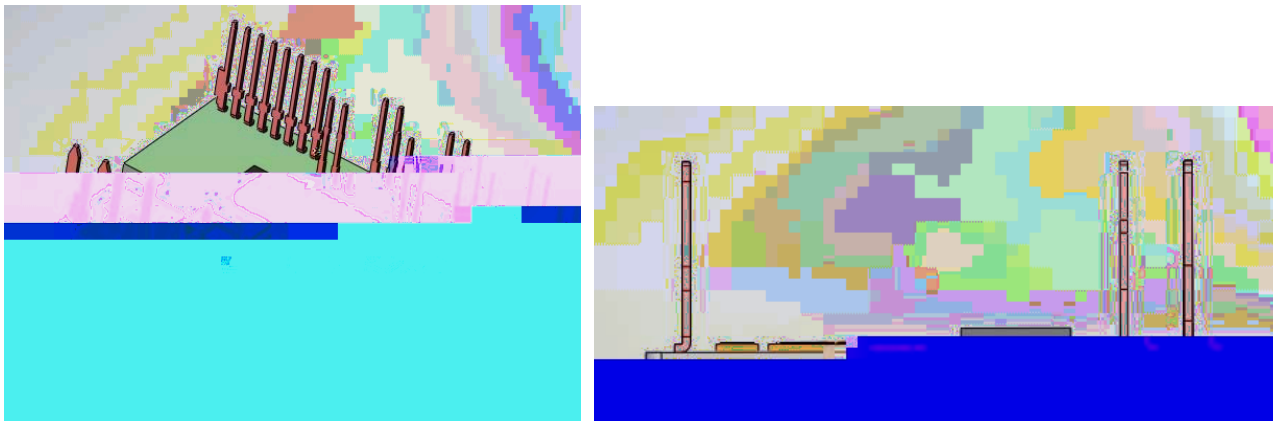


Figure 3-1. ID IPM Internal Structure

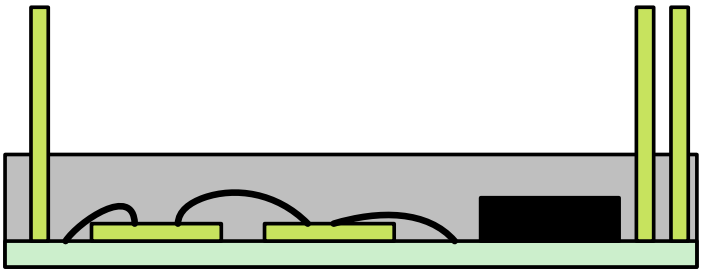


Figure 3-2. ID-IPM Package Cross Section

3.1.2 Driving and Protection Functions

Driving logic

- When the logic level of $IN_{(xH)}$ or $IN_{(xL)}$ is in high state then its corresponding IGBT will be “ON”. And when $IN_{(xH)}$ or $IN_{(xL)}$ is in low state then its corresponding IGBT will be “OFF”.
- Under-Voltage protection: if the input level of $V_{IN(xH)\ \&\ IN(xL)}$ is higher than $V_{th(on)}$ then IPM will work normally, If the input level of $V_{IN(xH)\ \&\ IN(XL)}$ is lower than $V_{th(off)}$, then IPM will shut-off its output.

Short circuit protection

- Usually the designer will use external shunt resistance to detect the injection DC-Link current to protect the load. When the current exceeds a preset SC trip level, it is judged as a short circuit state, and IPM will shut off its output immediately.
- Once the current is over the current limitation passing through the external shunt resistance. A fault pulse signal will output and the pulse duration will be determined by the capacitance of the capacitor connected between C_{FOD} and COM. After it is being outputted continuously for a certain period of time (depends on the capacitor), fault condition will be reset when the next input signal reaches the normal level.

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tightening on one side only. Figure 2-5 shows the recommended fastening order for mounting screws. In the first use screwdriver temporary fastening screws, then use screwdriver permanent fastening. Note that uneven mounting can cause the ID-IPM housing and molding compound to be damaged.



Figure 3-5. Recommended Fastening Order of Mounting Screws

The heat sink flatness (warp/concavity and convexity) on the module installation surface (refer to Figure 2-6), please follow the guidelines below in order to get effective heat-radiation when you want to enlarge the heat area.

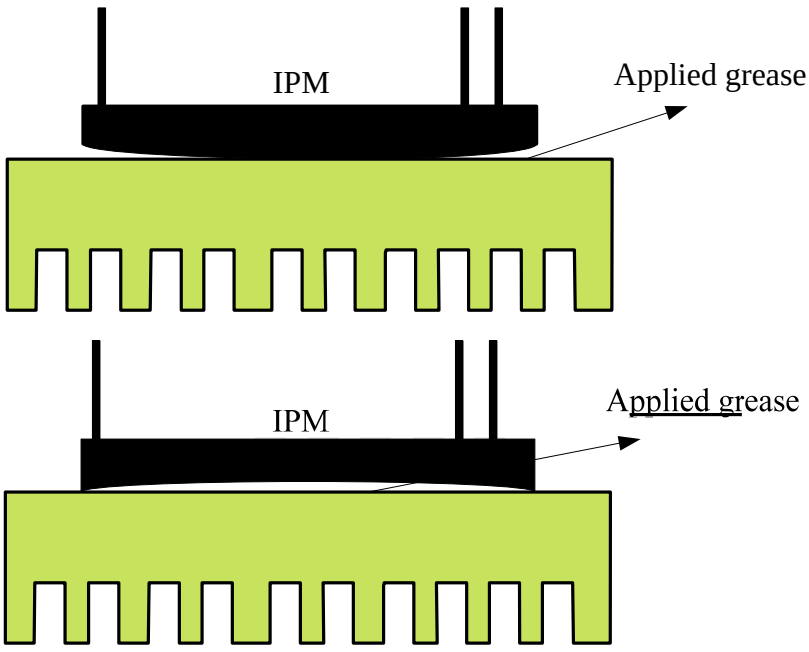


Figure 3-6. Heat Sink Flatness Specification

- Be sure cart surfaces that come into contact with device packaging are made of materials that will conduct static electricity, and are grounded to the floor surface with a grounding chain.
- To wear finger cots or gloves protected against static electricity if the human body comes into direct contact with a device,
- When humidity in the working environment decreases, the human body and other insulators can easily

Chapter 4 Applications

4.1 System Connection Diagram

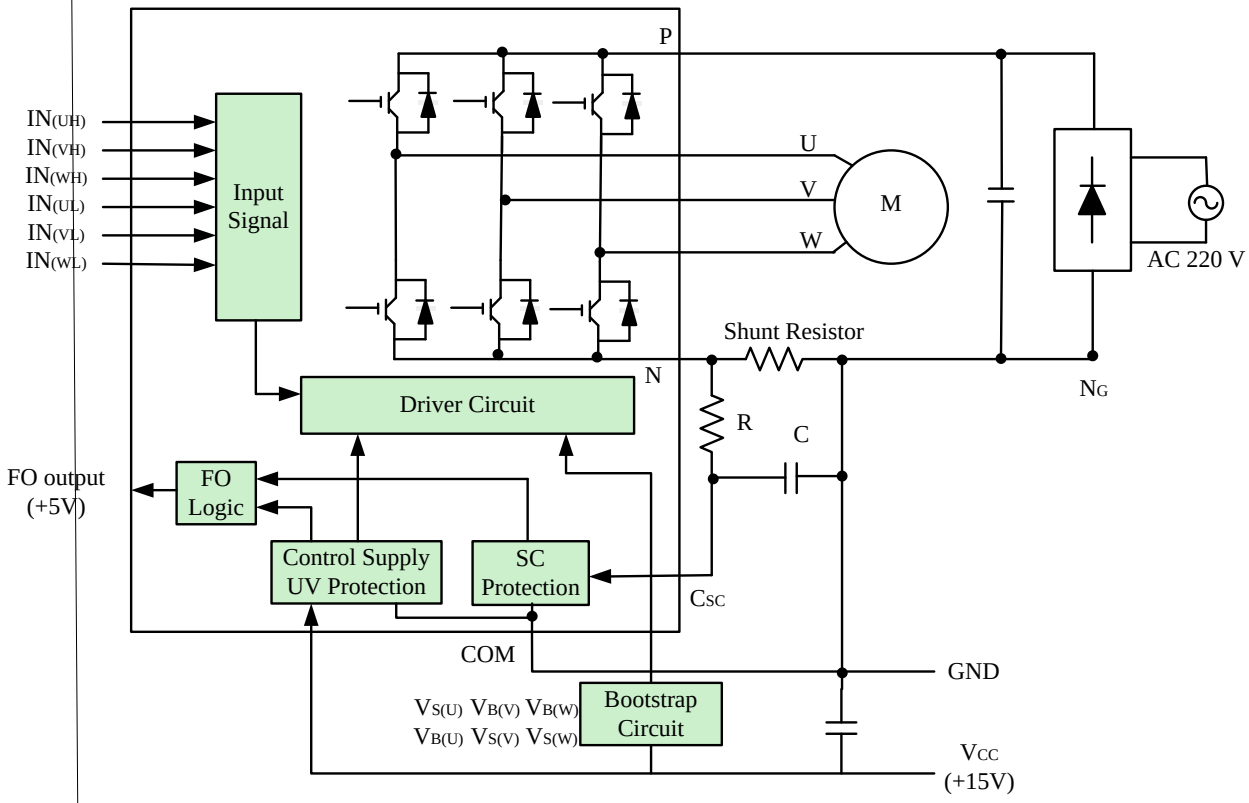


Figure 4-1. System Block Diagram of the IPM

4.2 Structure of Signal Input Terminals

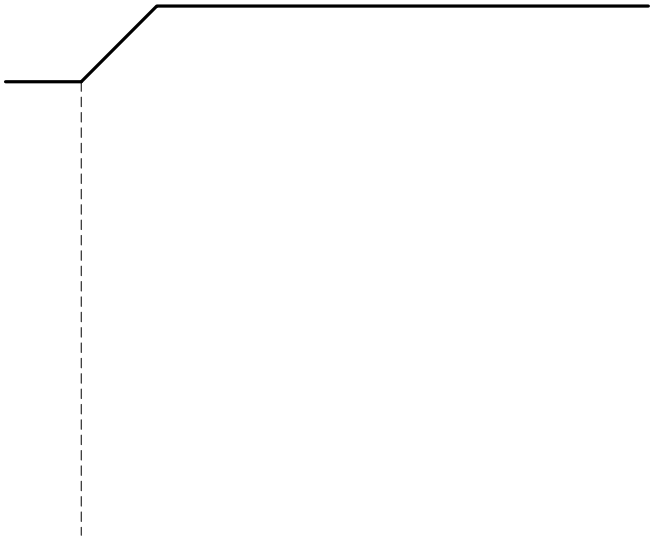
Note RC coupling at each input may be changed depending on the PWM control scheme used in the application and on the wiring impedances of the application's PCB.

Signal Input and Fault Output

The structure of IPM signal input terminals i-8.8(hac.to)-5.6(w)13.7(n i)-6.3(n)1(F)-4.3(i).4(gur)-8.8(e)]TJ27.4667 0 TD-.0015 Tc.017 T
utput i- an open coll ector type and it's rating i- 20.3V, 15V-c lass
or the fault output same as the input signals.

Table 4-1. Maximum Ratings of Input Signal and FO Pins Voltage

Item	Symbol	Condition	Ratings	Unit
Input signal voltage	$V_{IN(XH)}$ $V_{IN(XL)}$	Applied bethaween $IN_{(XH)}$ – COM $IN_{(XL)}$ – COM	-0.3 ~ +5	V



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Q_g = Gate charge of the high-side of the IGBT
f = Switching frequency
$I_{CBS(leak)}$ = Bootstrap capacitor leakage current
$I_{GE(leakage)}$ = Gate to emitter leakage current for the driver IC
Q_{LS} = Level shift charge required per cycle = 5nC(built in driver IC)

The bootstrap capacitor must be able to supply this charge Q_{BS}, and retain its full voltage. Otherwise, there will be a significant amount of ripple on the V_{BS} voltage, which could fall below the V_{BSUV} (under-voltage detection level). Hence, it is recommended that the charge in the C_{BS} capacitor be at least twice the above value. Due to the nature of bootstrap circuit operation, a low value capacitor can lead to overcharging, which could in turn damage the driver IC. The minimum bootstrap capacitor value can be obtained from the following equation (4.3). Recommend to put the experienced value from 10uF~22uF.

$$C_{BS} \geq \frac{Q_g + \frac{I_{GE(leakage)} + I_{CBS(leak)}}{f} + Q_{LS}}{\Delta V} \tag{4-3}$$

Where ΔV = the allowable discharge voltage of the C_{BS}.

Note that the following equation (4.4) should be used for a specific system application, with an extended period of application of the standstill mode of the PWM output, during the changing of the rotor direction.

$$C_{BS} \geq I_{BS} \times \Delta T / \Delta V \tag{4-4}$$

Where ΔT is the maximum ON pulse width of IGBT1 and I_{BS} is the drive current of the driver IC (depends on temperature and frequency characteristics), and ΔV is the allowable discharge voltage.

The bootstrap capacitor should always be placed as close to the pins of the IPM as possible. A separate ceramic capacitor close to the IPM would be essential if an electrolytic capacitor were used for the bootstrap capacitor. Using a ceramic or tantalum type for the bootstrap capacitor, it should be adequate for local decoupling.

4.3.4 Series Resistor Selection

A resistor R_{BS} must be added in series with the bootstrap (ID-Series IPM Application Note the series resistor relative to the value of the bootstrap capacitor should be chosen such that the RC time constant is equal to or greater than 10us. Note that if the rising dV_{BS}/dt is slowed down significantly, it could temporarily result in a few missing pulses during the start-up phase due to insufficient V_{BS} voltage.

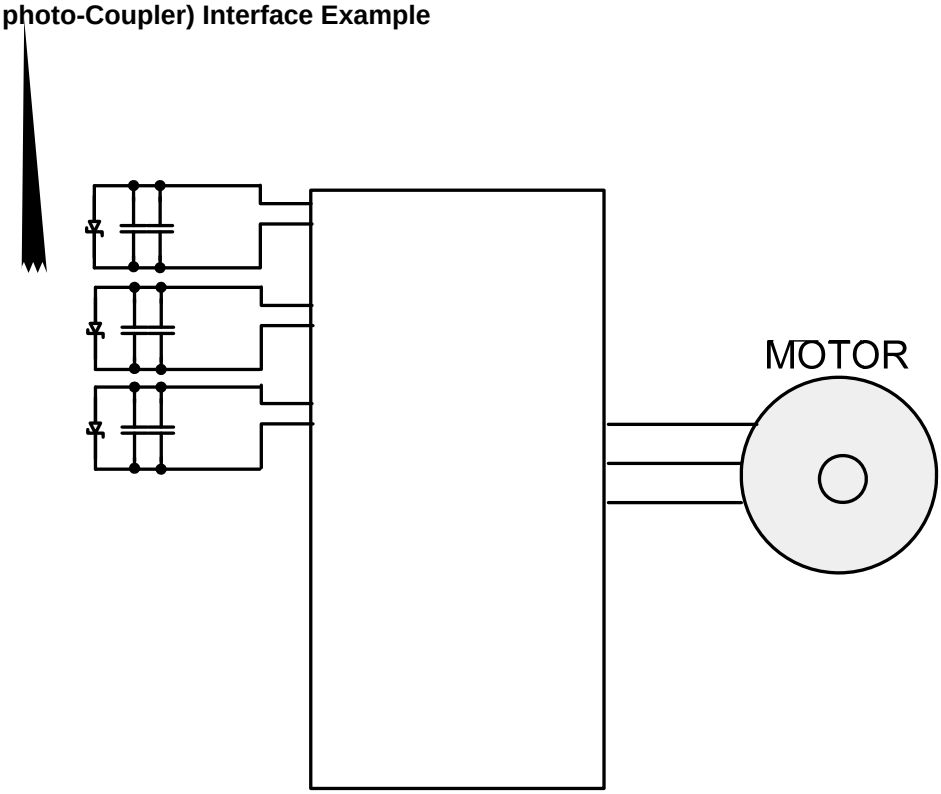
Resistor R_{BS} should be basically selected such that the time constant R_{BS} x C_{BS} will enable the discharged voltage ΔV being charged again into C_{BS} within the maximum ON pulse width of IGBT2, as show figure 4.7. However, if only IGBT1 has an ON-OFF-ON control mode, the time constant should be set so that the consumed charge during the ON period can be charged during the OFF period.

4.3.5 Bootstrap Diode Selection

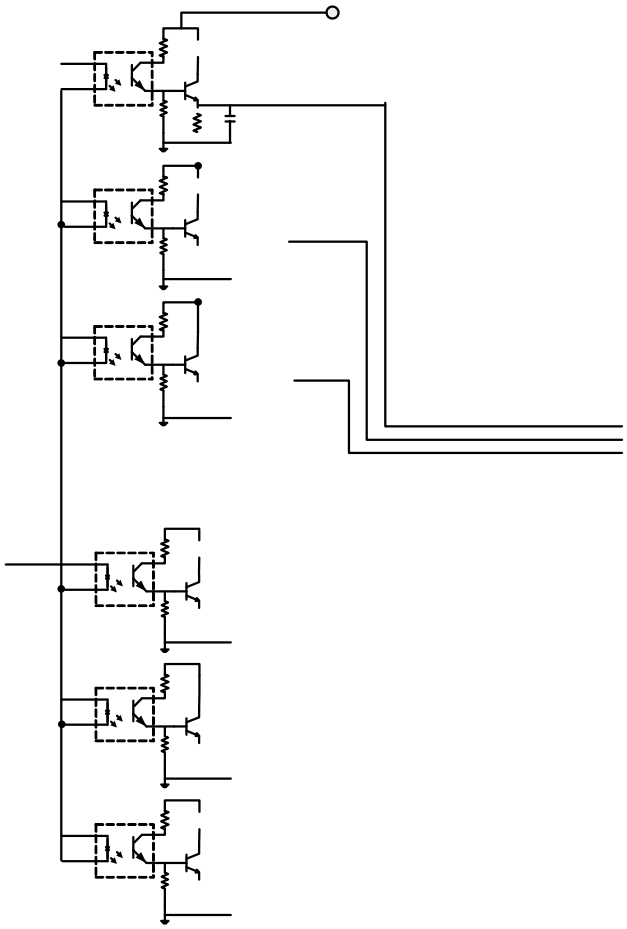
The bootstrap diode D_{BS} is used for blocking the inverter DC-link voltage when the high-side device is switched “ON. So the bootstrap diode with withstand-voltage more than 600V is recommended. It is also important that the diode should be an ultra-fast recovery device to minimize the amount of charge that is fed back from the bootstrap capacitor into the V_{CC} supply. Similarly, the high temperature reverse leakage current would be important if the capacitor has to store a charge for long periods of time.

4.4 Application Circuit and Recommended Parts

4.4.1 Direct Input (without photo-Coupler) Interface Example



4.4.2 Interface Example When a Photo-Coupler is Used



4.5 Input / Output Timing Diagram

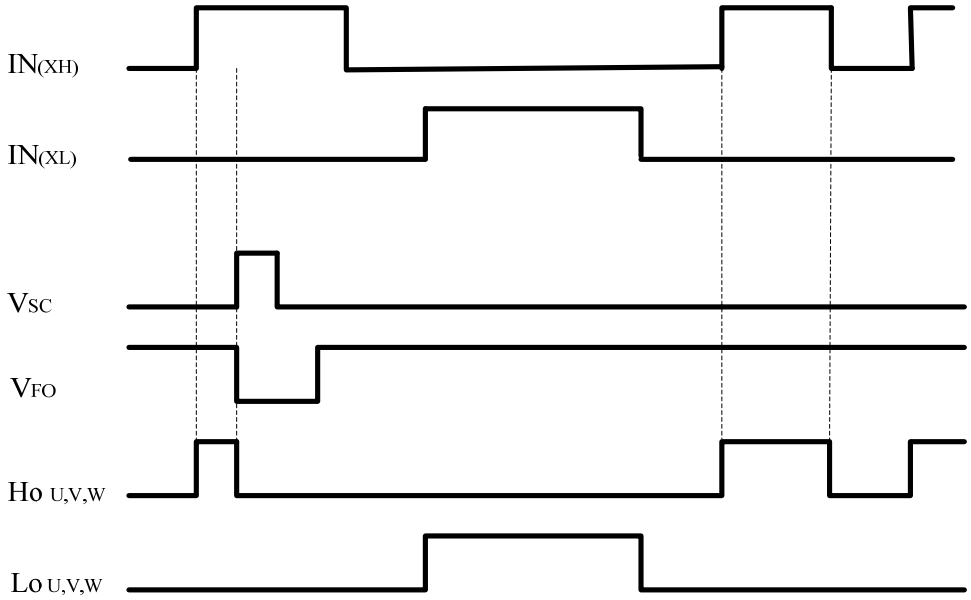
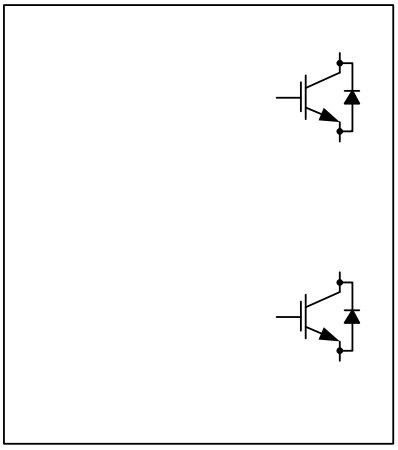


Figure 4-10. Input / Output Timing Diagram

Note The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.



VSC	IN(XH)	IN(XL)	U,V,W
0	1	0	DC Bus
0	0	1	Vce(sat)
0	0	0	0

4.6 Function and Protection Timing Charts

4.6.1 Timing Charts of Short Circuit Protection

(For the external shunt resistor and

4.6.2 Timing Charts of Under-voltage Protection

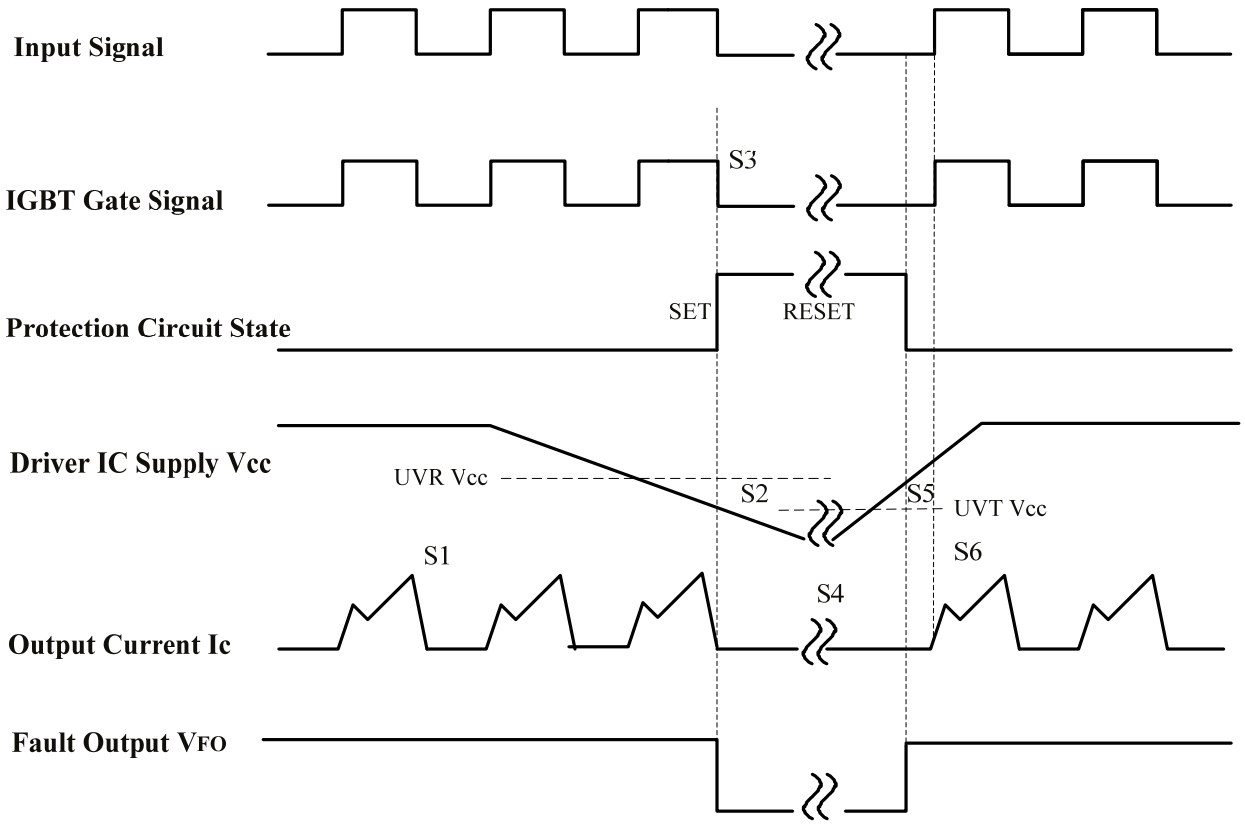


Figure 4-13. Timing Chart of Under-Voltage Operation

S1. Normal operation : IGBT ON and carrying current
S2. Under-voltage trip
S3. IGBT turns OFF inspire of control input condition
S4. FO timer operation starts : The pulse width of the FO signal is set by the external capacitor.
S5. Under-voltage reset
S6. Normal operation : IGBT ON and carrying current

4.6.3 Fault Output Loop



- Figure 4-14. shows the relationship between sensing resistor values and interrupted current values, based on various conditions including fluctuation range described in Table 4-6.

- In the actual design, the filter circuit would be necessary and the sensing resistor value should be evaluated.

Table 4-6. Specification for $V_{SC\ (ref)}$

Condition	Min.	Typ.	Max.	Unit
$V_{SC(ref)}$ specification at T_a=25 (Typ.)	0.45	0.50	0.55	V

Example

Sample NO. ID20FT06A1S (20A/600V)

The maximum recommended short-circuit trip current is 1.7 times the nominal IC rating of the module

Isc(max) = Ic(rating) × 1.7 = 20 × 1.7 = 34A

The minimum allowable shunt resistance is determined by requiring that the protection must operate at Ic = 34A, even if the modules short-circuit detection reference level (Vsc(ref)) is at its maximum. Referring to Table 4-6. for Vsc(ref) the minimum shunt resistance is

Rshunt(min) = Vsc(ref)max / Isc =0.55 / 34 = 16.1 mΩ

If the tolerance of the shunt resistor is 5% then the possible range is

Rmin = 16.1 mΩ, Rtyp = 17.0 mΩ, and Rmax = 17.8 mΩ

The typical short-circuit trip current is

Isc(typ) = Vsc(ref)typ / Rtyp = 0.46 / 0.017 = 27.06A

The minimum short-circuit trip current is

Isc(min) = Vsc(ref)min / Rmax = 0.37 / 0.0178 = 20.78A

Therefore, the range for short-circuit trip current is from 20.78A to 27.06A.

4.6.5 Filter Circuit Setting (RC Time

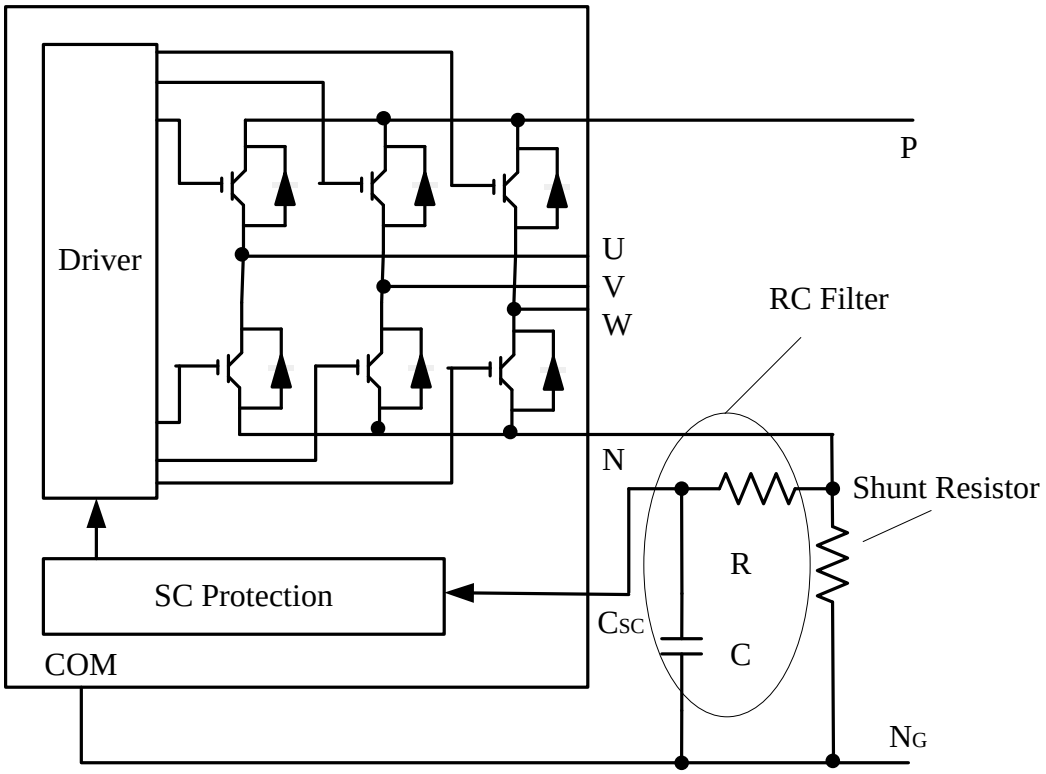


Figure 4-15. Example of External RC Filter Circuit

Figure 4-16 shows the example of external SC protection circuit. If the output current exceeds the SC trip level, all the gates of each IGBT are interrupted and the fault signal FO is outputted. The system operation should be stopped immediately when the fault output signal is pulled low.

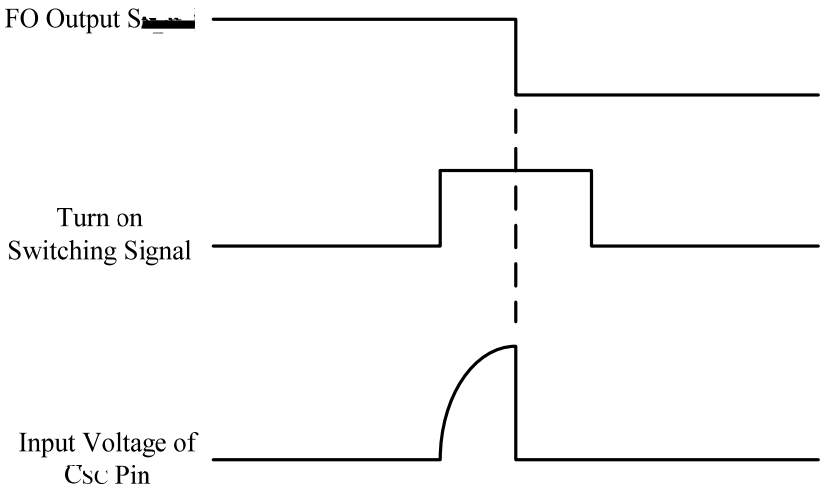


Figure 4-16. SC protection waveform

• Characteristics of RC Filter Circuit

When the RC filter circuit is connected, it can prevent the noise on the shunt resistor to make the SC protection

malfunction. The RC filter circuit immediately interrupts short-circuit currents due to its characteristics (shown in Figure4-17.) Figure 4-8 and Figure 4-9 show the recommended schemes for the different application of signal input. The RC time constant is determined depending on the applying time of noise interference and the withstand voltage capability of the IGBT.

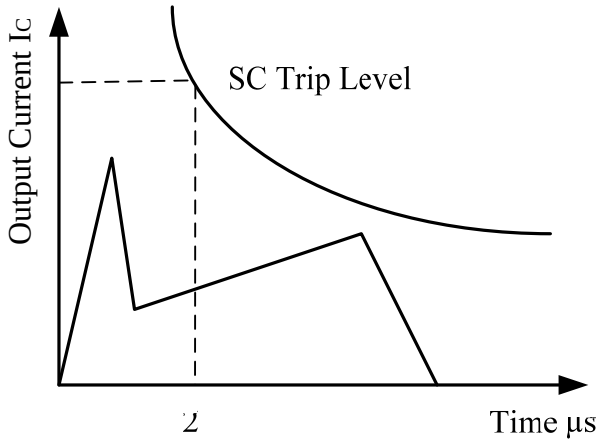


Figure 4-17. Characteristics of RC Filter Circuit

• **Setting of RC Time Constant**

An RC filter (R, C) should be 13.34 standard the PM CI.N pint s9 show

. Thfilter(,( )]TJ 41.6269 -1.5569 TD .0002 Tc 02124 Tw [RC)ae delaly t prteoe

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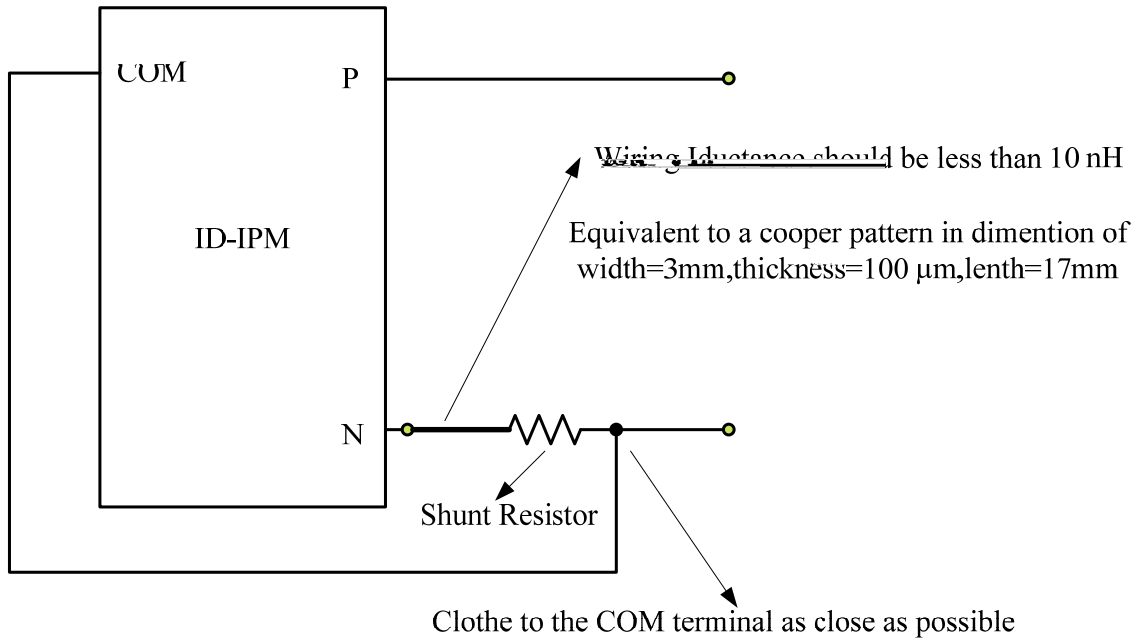

Figure 4-19. Recommend Wiring of Shunt Resistor

4.6.7 Parallel Connection

Figure 4-20 shows the circuit of parallel connection of two ID IPMs.

Rout H-loop and L-loop indicate the gate charging path of low-side IGBT in the ID IPM No.2. If the rout is too long, gate voltage might drop due to large voltage drop on the wiring, which will result a bad effect to the second IPM operation (Charging of bootstrap capacitor for high-side is similar, too.).

In addition, noise might easily impose to the wiring impedance. If there are many ID IPM parallel connection. COM pattern becomes long and the influence to other circuit (power supply, protection circuit etc.) by the fluctuation of COM potential is conceivable, therefore parallel connection is not recommended.

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Table 4-7. Protection table

V_{CC}	V_{BS}	V_{SC}	V_{FO}
< U_{VCC}	X	X	0
15V	< U_{VBS}	0	0
15V	15V	0	H imp
15V	15V	> V_{trip}	0

Note A shoot-through prevention logic prevents $L_{O1,2,3}$ and $H_{O1,2,3}$ for each channel from turning on simultaneously.
Note U_{VCC} is not latched, when Vcc U_{VCC}, FO returns to high impedance.
Note Over-current protection are latched protection and V_{FO} will turn high impedance after the fault condition recovery.

Chapter 5 Safe Operating Area

5.1 Safe operating area of the IPM

5.1.1 Definition of SOA

By built-in gate drive, under-voltage

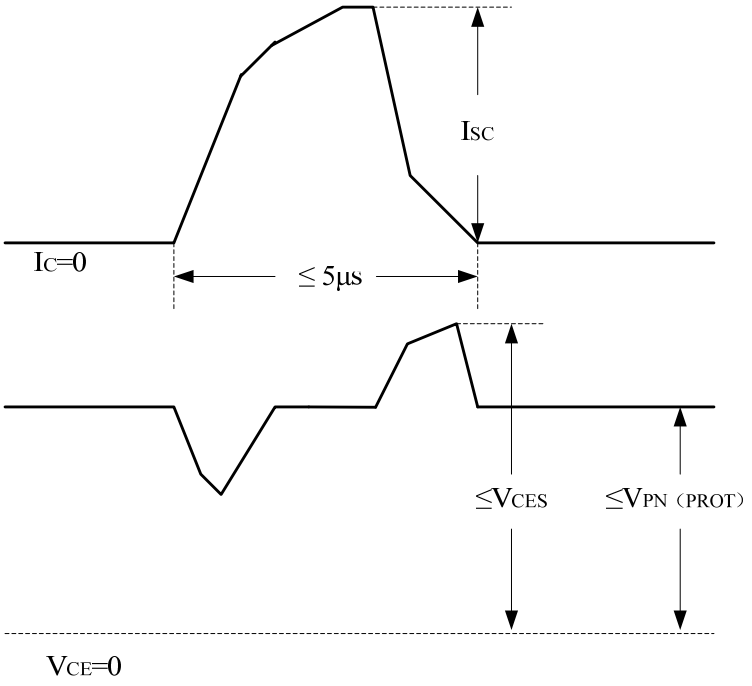
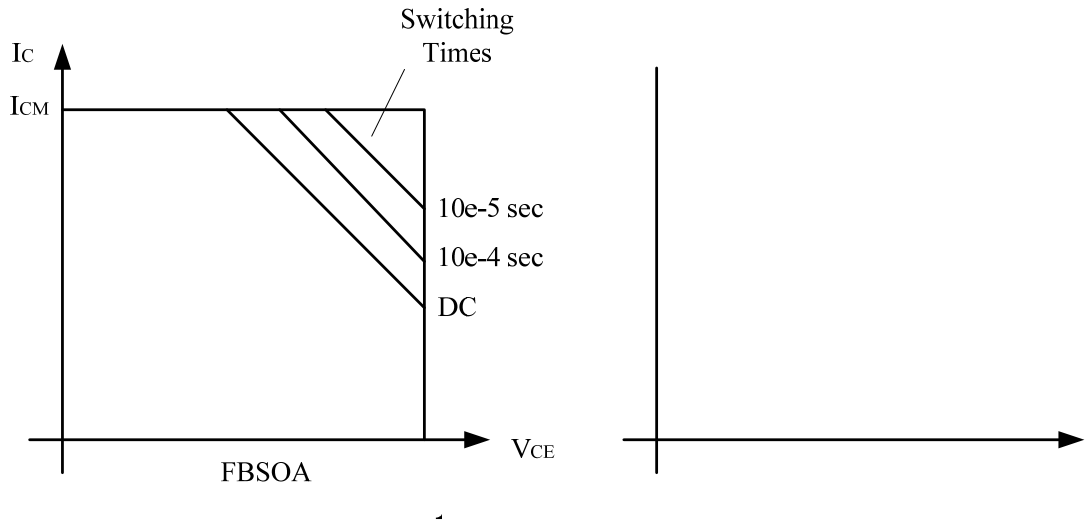


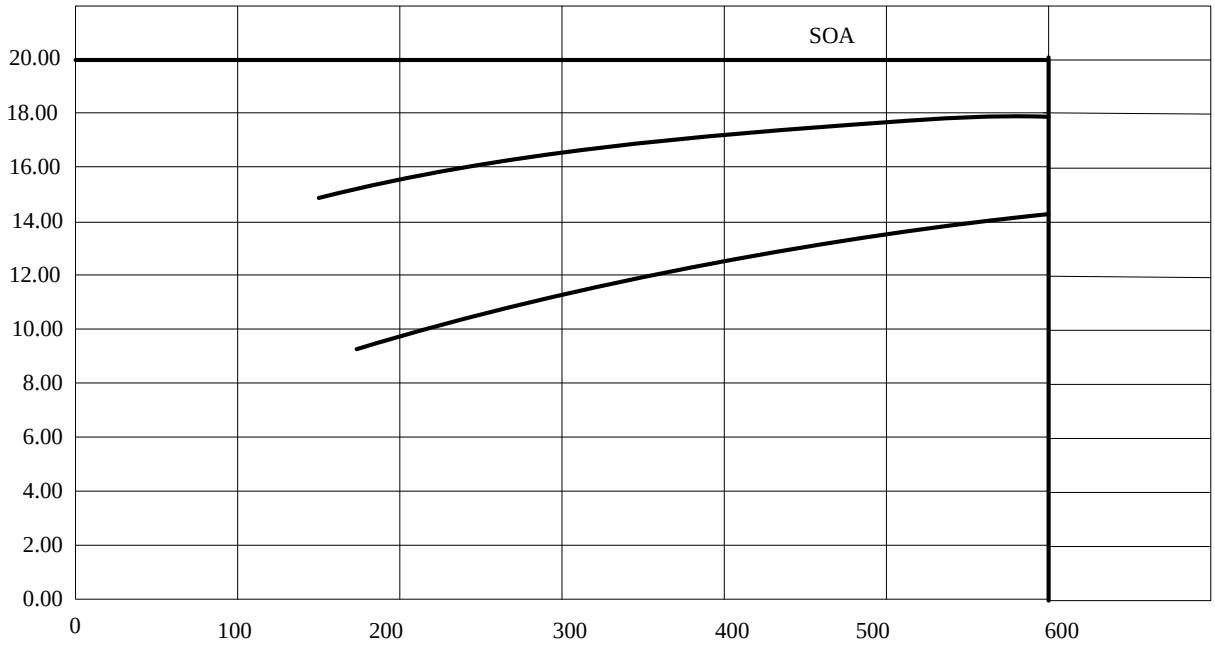
Figure 5-2. SOA for Short-circuit

5.1.2 Switching Operation

In fact, the V_{CES} represents the 600V voltage rating of the IGBTs incorporated into the IPM. But subtracting the surge voltage generated by the stray inductance of the PCB trace and the internal wire bonding of the IPM. Moreover, subtracting from V_{PN}(Surge) the surge voltage generated by the stray inductance between the IPM and the DC-link capacitor is V_{PN} (Surge), please refer to the data sheet for the rated surge voltage .

1. FBSOA – Turn on transition (Power dissipation limited)
2. RBSOA – Turn off transition (Latch-up spec)




SOA
20.00
18.00
16.00
14.00
12.00
10.00
8.00
6.00
4.00
2.00
0.00
0
100
200
300
400
500
600

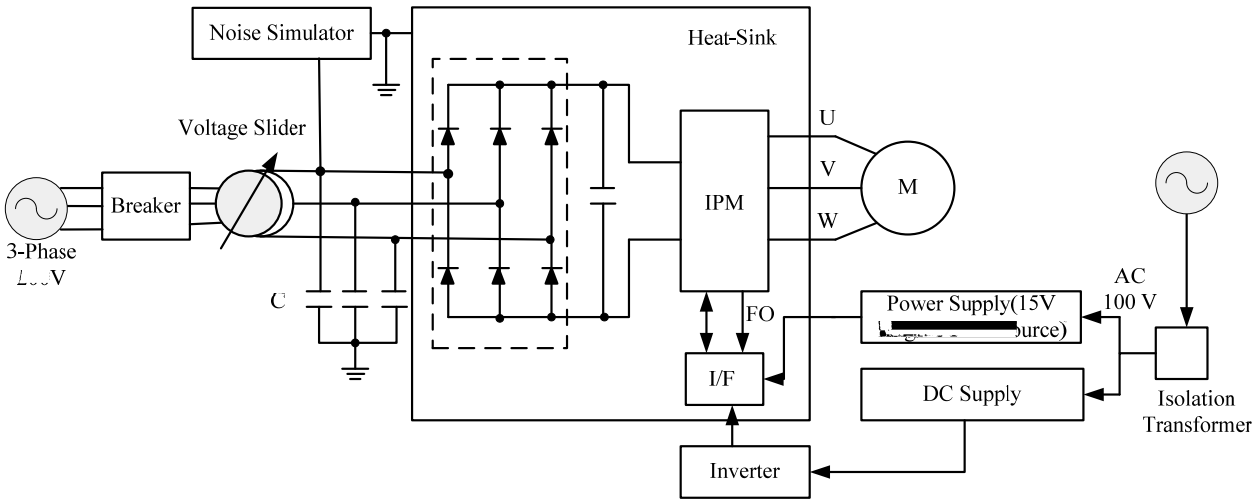


Figure 5-5. Noise test circuit

Note

C AC line common-mode filter 4700pF

PWM signals are inputted from microcomputer both directly and through opto-coupler

15V single power-source drive

Test is performed for both IM and DCBLM motors

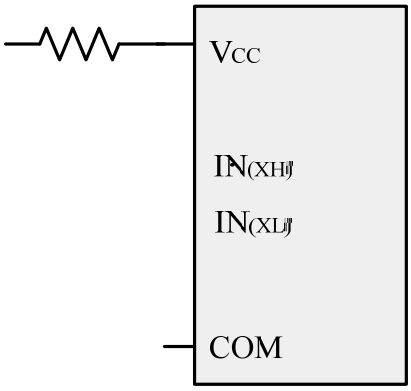
Test conditions

VCC=300V,VD=15V,Ta=25 ° C, no load.

50ns~1us wide pulses are applied at a random point each 60Hz cycle.

5.3 ESD withstand capability

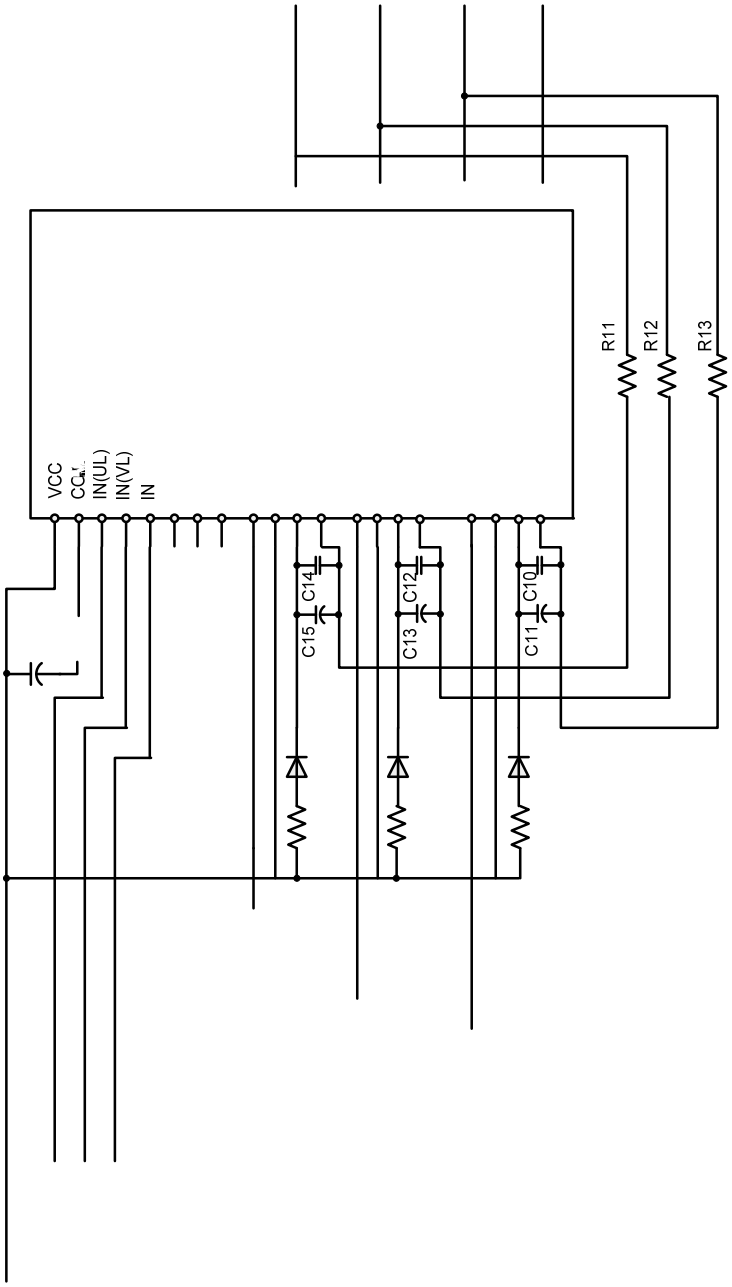
ID-IPM has been confirmed to be with ± 250V or more withstand capability under the above evaluation circuit.



Chapter 6 Reference Design

6.1 Demo board introduction

- **Demo board schematic**



- **Bill of Materials**

Table 6-1.Demo-Board B.O.M List

Used	Part Type	Rating	Characteristics	Definition
1	C1	1 nF	Ceramic Capacitor	Low-Side Pull-Down Capacitor
2	C2	1 nF	Ceramic Capacitor	Low-Side Pull-Down Capacitor
3	C3	1 nF	Ceramic Capacitor	Low-Side Pull-Down Capacitor
4	C4	1 nF	Ceramic Capacitor	High-Side Pull-Down Capacitor
5	C5	1 nF	Ceramic Capacitor	High-Side Pull-Down Capacitor
6	C6	1 nF	Ceramic Capacitor	High-Side Pull-Down Capacitor
7	C7	1 nF	Ceramic Capacitor	+5V Bias Voltage Bypass Capacitor
8	C8	33 nF	Ceramic Capacitor	Capacitor for Selection of Fault Out Duration
9	C9	1 nF	Ceramic Capacitor	Bypass Capacitor for Current Sensing
10	C10	100 nF	Ceramic Capacitor	Bypass Capacitor for Bootstrap Supply (Phase U)
12	C11	6.8 uF 35 V	Electrolytic Capacitor	Bootstrap Capacitor (Phase U)
13	C12	100 nF	Ceramic Capacitor	Bypass Capacitor for Bootstrap Supply (Phase V)
14	C13	6.8 uF 35 V	Electrolytic Capacitor	Bootstrap capacitor (Phase V)
15	C14	100 nF	Ceramic Capacitor	Bypass Capacitor for Bootstrap Supply (Phase W)
16	C15	6.8 uF 35 V	Electrolytic Capacitor	Bootstrap capacitor (Phase W)
17	C16	220 uF 35V	Electrolytic Capacitor	+15V Bias Voltage Source Capacitor
18	C17	100 nF 630V	Film Capacitor	Snubber Capacitor to Suppress the Spike-Voltage
19	C18	1uF 35V	Ceramic Capacitor	+15V Bias Voltage Bypass Capacitor
20	R1	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (UL)
21	R2	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (VL)
22	R3	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (WL)
23	R4	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (UH)
24	R5	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (VH)
25	R6	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (WH)
26	R7	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (Fault-out)
27	R8	20Ω 1/4 W	Carbon Film Resistor	Bootstrap Resistor (Phase U)
28	R9	20Ω 1/4 W	Carbon Film Resistor	Bootstrap Resistor (Phase V)
29	R10	20Ω 1/4 W	Carbon Film Resistor	Bootstrap Resistor (Phase W)
30	R11	5.6Ω 1/4 W	Carbon Film Resistor	Emitter Resistor for Switching
31	R12	5.6Ω 1/4 W	Carbon Film Resistor	Emitter Resistor for Switching
32	R13	5.6Ω 1/4 W	Carbon Film Resistor	Emitter Resistor for Switching
33	R14	4,7KΩ 1/8 W	Carbon Film Resistor	Pull-up Resistor (Fault output)

35	R16	20mΩ 5 W

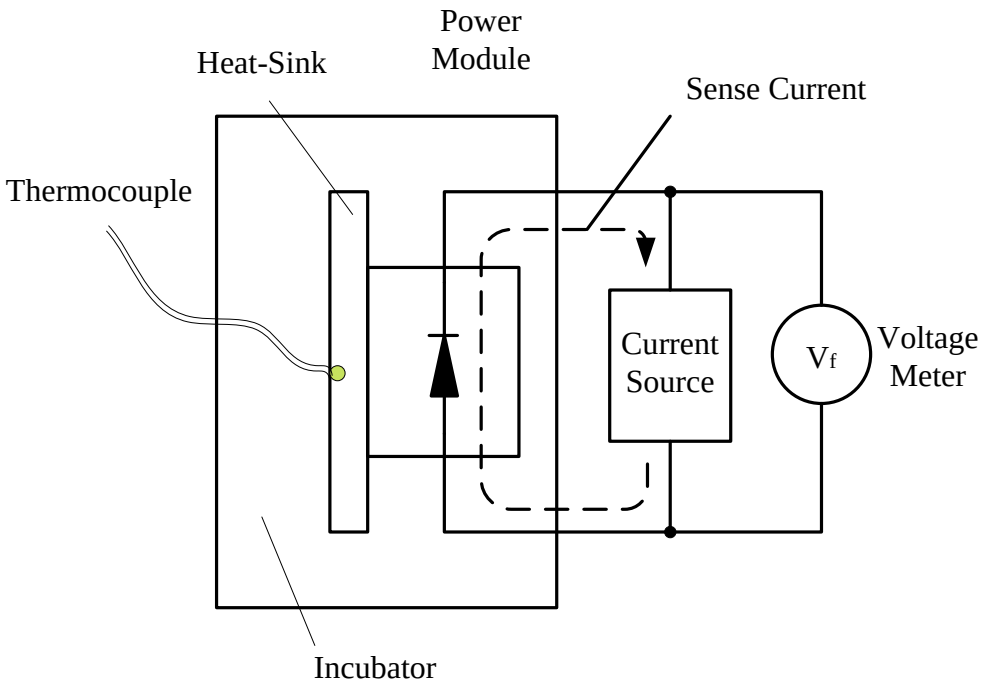
6.2 Layout Guide-line

- It is recommended that the wiring of the DC- link power path be as short as possible.
- To suppress surge voltage, a non-inductive snubber capacitor should be mounted as close to P and GND (shunt resistor's return pins) as possible.
- The wiring of N terminal and shunt resistors should be as short as possible and shunt resistors' pin connected DC-link GND also should be as short as possible.
- To prevent the input signals oscillation, an RC coupling at each input is recommended, and the wiring of each input should be as short as possible.
- To minimize the pattern impedance, it is recommended that the bootstrap current path be as short as possible.
- FO output is open collector type. The signal line should be pulled up the positive side of the 5V power supply with approxima(o)-.6(ub/TT15kTT11 1 T710.02 0 043110 Tc.0575)TjTja1T11 1 Tf.7425 099.0004 Tc0513 T217( )-778..2

Where T_A = Ambient temperature [ ]

$R_{\theta JA}$

The Electrical Test Method (ETM) uses the forward voltage dropped of a junction as the temperature sensitive parameter and is variously known as the “diode-forward-drop” method from original applications with power diodes and bipolar power transistors. It is based on a temperature and voltage dependency exhibited by all semiconductor diode junctions. This relationship can be measured and used to compute the semiconductor junction temperatures in response to power dissipation in the junction region. The voltage-temperature relationships are an intrinsic electro-thermal property of semiconductor junctions, and are characterized by a nearly linear relationship between forward-biased voltage drop and junction temperature when a constant forward-biased current is applied. This constant current is called the “sense current” (also “measurement current”). This voltage drop of the junction is called Temperature sensitive Parameter (TSP). Figure 7-2 illustrates the concept of measuring this voltage versus junction temperature relationship in for a diode junction. The device under test (DUT) is embedded in hot fluid to heat DUT up to desired temperatures.



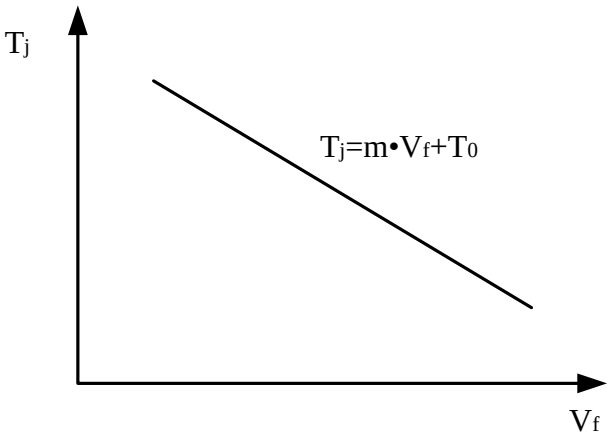


Figure 7-3. Typical Example of a TSP Plot with Constant Sense Current

The relationship between the junction temperature and voltage drop can be expressed mathematically as in the calibrating relationship,

$$T_J = m * V_f + T_0 \tag{7-5}$$

The slope, “m” (deg C/volt) and the temperature ordinate-intercept, “T_0” are used to quantify this straight line relationship. The reciprocal of the slop is often referred as the “K factor” expressed in units of mV/ . In this case, V_f is the “temperature sensitive parameter” (TSP). For semiconductor junctions, the temperature/voltage slope of the calibrating straight line is always negative, i.e., the forward conduction voltage decreases with increasing junction temperature. Once the slope and intercept have been determined, the junction is calibrated for use as a temperature sensor. The voltage generated in response to the applied sense current can then be used to compute the junction temperature using the calibrating relationship (Equation 7-5).

7.3 Measurement Procedures

This section covers the application of the electrical test method to a variety of functional device categories. These categories are determined by the electrical design of the die utilized in the specific component under test.

Thermal Test Die

Thermal test dice are specifically designed for thermal characterization of integrated circuit packages. These dice are available in a variety of sizes and can be mounted into any desired package to create a thermal test vehicle. They have been designed to offer electrically independent power dissipation and electrical measurement of junction temperature. The thermal die test method is illustrated schematically in figure 7-4. Thermal dice offer accurate thermal characterization with a minimum of measurement hardware. The sense diode voltage can be directly measured with a voltmeter and the associated junction temperature computed (Equation 7-5) using predetermined

calibrating parameters.

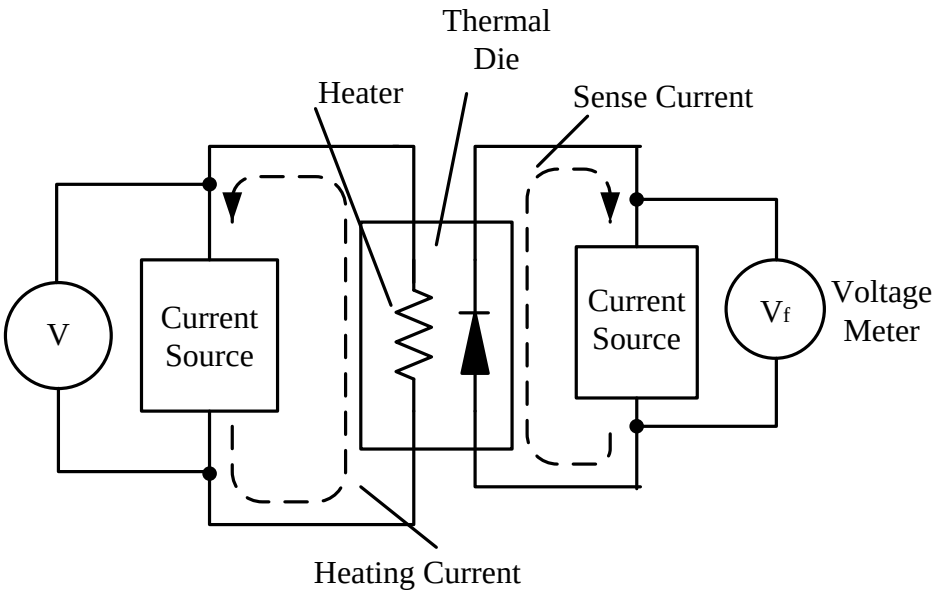


Fig. 7-4 Illustration of Thermal Test Die Test Method Concept

Active Dice

Active or functional dice are often used as the ultimate test for component thermal characterization. The primary feature that distinguishes active die from thermal die is that heat dissipation is not electrically independent from temperature sensing and that the die is designed to perfor

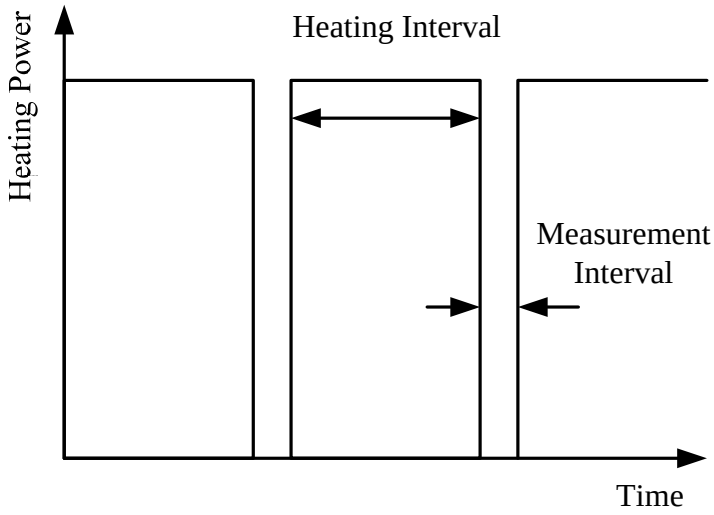
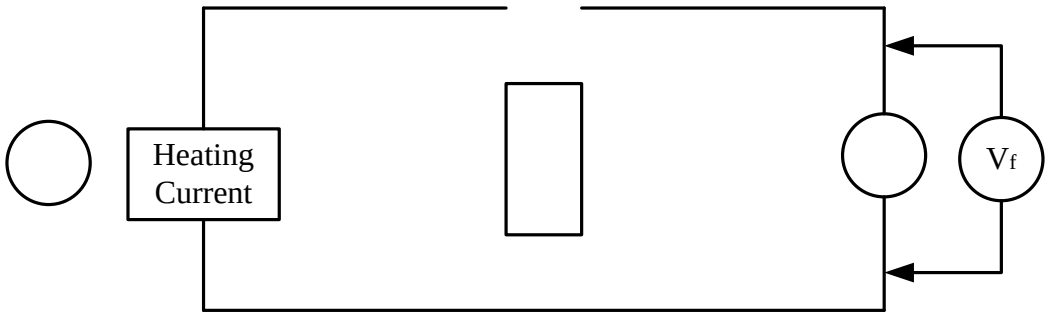


Fig. 7-5 Graphic of Illustration of the Heating and Measurement Intervals

The test procedure for testing a rectifier diode provides an excellent example of some common issues associated with application of the electrical method to active die testing. Figure 7-6 schematically illustrates the electrical test method for a rectifier diode.



Chapter 8 Power Loss and Dissipation

An IPM consists of Driver IC, IGBTs and Diodes .The su

Prerequisites:

For approximate power loss calculations, the following prerequisites are necessary

1. Sine waveform current output PWM control VVVF inverter
2. PWM signals based on the comparison of sine waveform and triangular waveform
3. Three-phase PWM control VVVF inverter for sine-wave current output
4. Output current in ideal sin-waveform
5. The typical forward characteristics are approximated by the following linear equation for the IGBT and the Diode

   $V_{ce(sat)} = V_o + R_i \times i_c$

   $V_F = V_D + R_d \times i_F$

   V_o = Threshold voltage of IGBT V_D = Threshold voltage of diode

   R_i= on-state slope resistance of IGBT R_D = on-state slope resistance of diode

   Where Vce(sat) and VF are the saturation voltage of IGBT and the saturation voltage of diode, as displayed in figure 8-1 the output characteristics of IGBT and Diode have been approximated based on the data contained in the IPM spec.

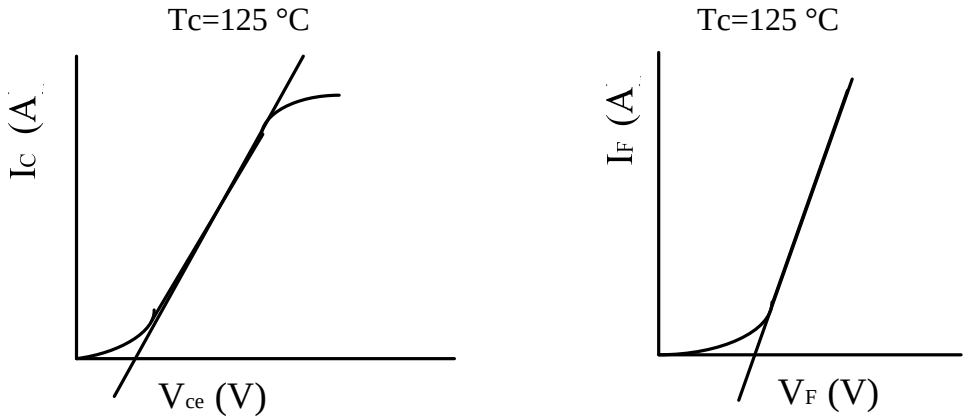


Figure 8-2 Output Characteristics of IGBT and Diode

6. Output current is given by sin x • I_{CP} and it not have ripple current
7. Assume inductive load is ideal and Load power factor for output current is cosθ
8. IGBT saturation voltage Vce(sat) is in proportion to the collector current IC
9. Diode forward voltage drop V_F is in proportion to the forward current Irr

The conduction loss in IGBT and FWD can be calculated as follows:

$$P_{IGBT} = \frac{1}{2} DT \quad \frac{2\sqrt{2}}{\pi} I_M V_O + I_M^2 R$$

$$P_{Diode} = \frac{1}{2} DF \quad \frac{2\sqrt{2}}{\pi} I_M V_D + I_M^2 R$$

DT, DF: Average conductivity of the IGBT and Diode at a half wave of the output current.

8.2 Switching Loss and Calculation Method

Switching loss can be calculated form turn on/off time and over-voltage / current characteristics.

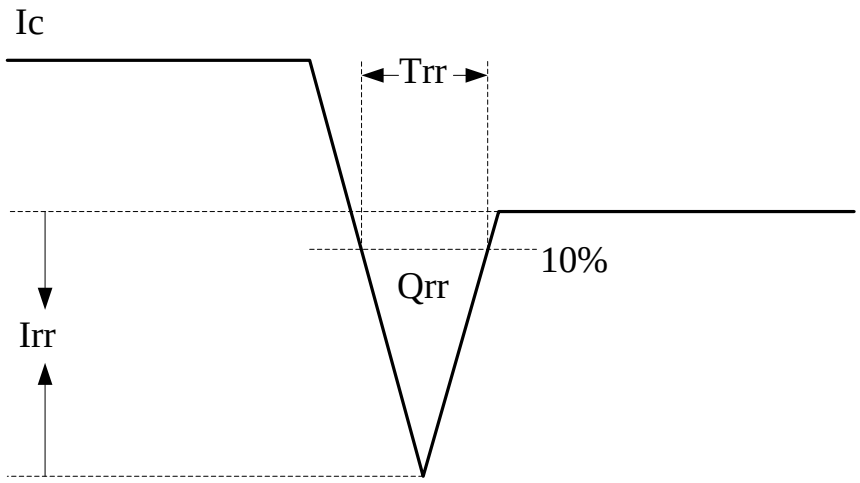


Figure 8-3 Diode loss

Therefore, the loss of diode is idealized as shown in Figure 8-3 and recovery occurs in the middle of output current period. Therefore the formula is below:

$$P_{SW(Diode)} = \frac{1}{2} \times f_c \times \frac{I_{rr} \times t_{rr} \times V_D}{4}$$

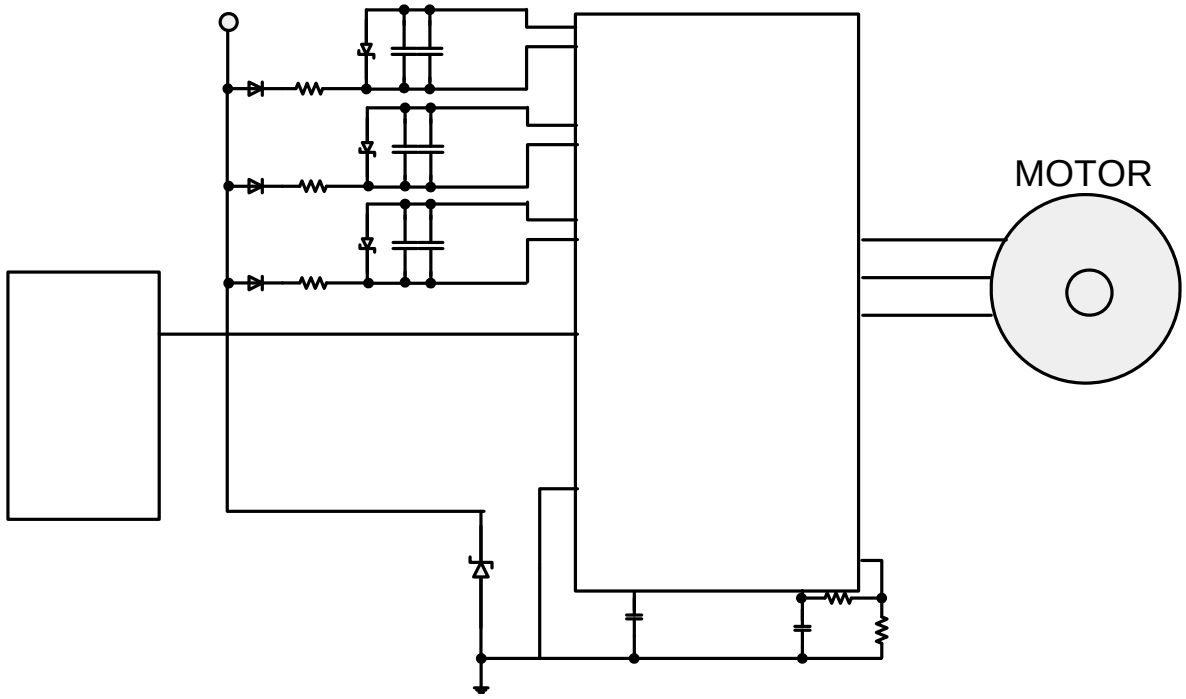
IGBT power loss = $P_{IGBT} + P_{SW(IGBT)}$

Diode power loss = $P_{Diode} + P_{SW(Diode)}$

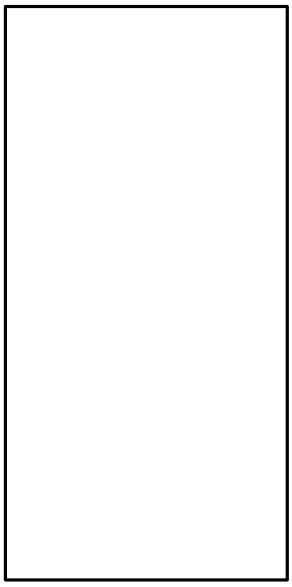
Chapter 9 Appendix Document

9.1 F.A.Q for Starpower ID IPM

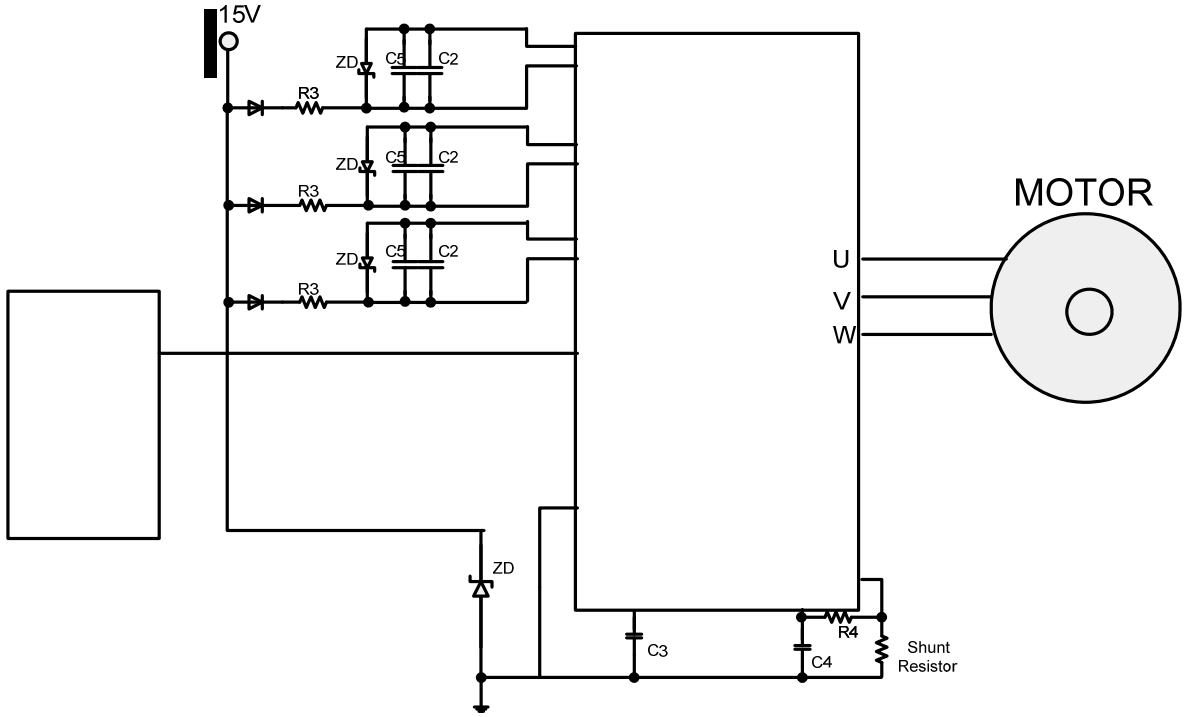
1) Circuitry reference design for application



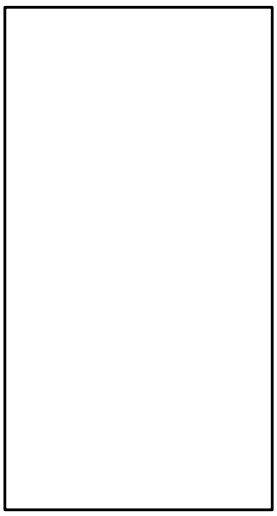
2) Can not start up the system after adopt IPM, or system shut-off immediately after start up.



3) MCU can not accept the fault signal from IPM for over loading testing.



9.2 Divided negative dc-link terminals for current sensing applications



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Chapter 10 Contact Information

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